UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,979	01/02/2004	Dong-Ho Lee	9903-074	5476

20575 7590 09/22/2005

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,979	LEE, DONG-HO	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 21-2620* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 08/16/05. These drawings are acceptable.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 21-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Recited the limitation 'wherein the first and second chip scale package have substantially a same width and substantially a same length', the description had been carefully reviewed, but failed to provide the support for such limitation.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4, 8, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pub 2002/0124518 to Karnezos.

Regarding claim 1, Karnezos discloses in fig. 5A a stack package including two or more area array type chip scale packages 400/500 [0097] [0099], each chip scale package comprising: a substrate 412 [0097], a plurality of ball land pads 423 [0097] formed on a lower surface of the substrate 412, a plurality of circuit patterns 423 formed on the lower surface of the substrate 412 and electrically connected to the ball land pads 423; and one or more chips 414 installed on an upper surface of the substrate 412 and electrically connected to the circuit patterns 423, wherein each chip scale package 400 of an adjacent pair of chip scale packages 500 is attached to the other in a manner where the ball land pads 523 [0099] of the upper stacked chip scale package 500 face in the opposite direction as the ball land pads 423 of the lower stacked chip scale packages 400, and wherein the circuit patterns 523 [0099] on the lower surface of the substrate of the upper stacked chip scale package 500 are electrically connected to those the circuit pattern 423 on the lower surface of the substrate of the lower stacked chip scale package 400, fig. 5A.

Regarding claim 4, Karnezos discloses the stack package according to claim 1, wherein a hole 422 [0097] is formed in the substrate of each chip scale package 400,

and the chip is electrically connected to the circuit patterns by bonding wires 416 [0098] passing through the hole, fig. 5A.

Regarding claim 8, Karnezos discloses the stack package according to claim 1, wherein a plurality of solder balls 418 [0098] is formed on the ball land pads 423 of the lowest stacked chip scale package 400, fig. 5A.

Regarding claim 11, Karnezos discloses the stack package according to claim 1, wherein a plurality of connection pads 421 are formed on the outside of the region of the substrate 412 on which a plurality of ball land pads 423are formed, and electrically connected to the circuit patterns 423.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-3, 5-7, 9-10, 12-13, 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub 2002/0124518 to Karnezos. In view of US Pub. 2004/0150107 to Cha et al.

Regarding claims 2-3, Karnezos discloses the stack package according to claim 1, wherein the circuit patterns 523 of the upper stack chip scale package 500 are electrically connected to the circuit patterns 423 of the lower stacked chip scale package.

But, Karnezos does not disclose the upper chip package and lower chip package are electronically connected by connecting boards, wherein each connecting board comprises a flexible film and wiring patterns formed on the film.

However, Cha discloses the stack package wherein the upper chip package 110A and lower chip package 110B are electronically connected by connecting boards 120, fig. 2, wherein each connecting board 120 comprises a flexible film 124 and wiring patterns 122 formed on the film [0078]. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the connecting board teaching of Cha with Karneos's device, because it would have increased the electrical feature of the stacked BGR package and improved the bonding force of a substrate bonding part of older ball as taught by Cha [0040] [0041].

Regarding claims 5-6, Karnezos discloses the stack package wherein the chip 414 is protected by a first encapsulating part 417 [0098],

But Karnezos does not disclose the stack package wherein a plurality of bonding pads of each chip scale package are formed on the central region of the chip and exposed through the hole, and wherein one end of each bonding wire 416 is attached to a corresponding bonding pad of the chip, and wherein the bonding pads and the bonding wires are protected by a second encapsulating part.

However, Cha discloses disclose the stack package in fig. 1 wherein a plurality of bonding pads (where 3 is attached) of each chip scale package 10 are

formed on the central region of the chip and exposed through the hole, and wherein one end of each bonding wire 3 is attached to a corresponding bonding pad of the chip, and wherein the chip 1 is protected by first encapsulating part 6 and the bonding pads (where 3 is attached) and the bonding wires 3 are protected by a second encapsulating part 5 [0007]. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the connecting board teaching of Cha with Karneos's device, because it would have increased the electrical feature of the stacked BGR package and improved the bonding force of a substrate bonding part of older ball as taught by Cha [0040] [0041].

Regarding claim 7, Karnezos discloses the stack package according to claim 6, wherein each chip scale package of an adjacent pair 500 of chip scale packages is attached to the other by an adhesive [0101] applied on the first encapsulating part 417, fig. 5A.

Regarding claims 9-10, 12-13, Karnezos discloses the stack package according to claim 1, wherein a single chip scale package is stacked on, and electrically connected through a plurality of solder balls 418 to adjacently stacked chip scale packages 500.

But Karnezos does not disclose the chip scale package is coupled by connecting boards, wherein both end of the connecting board at which the connecting board is attached to the connection pads are bent.

However, Cha discloses the stack package wherein the chip scale package in fig. 2 is coupled by connecting boards 120, wherein both end of the connecting board 120 at which the connecting board is attached to the connection pads are bent. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the connecting board teaching of Cha with Karneos's device, because it would have increased the electrical feature of the stacked BGR package and improved the bonding force of a substrate bonding part of older ball as taught by Cha [0040] [0041].

Regarding claims 21-26, as discussed in the claims 1-13 above Karnezos discloses all the limitation of claim 21, except the first and second chip scale package have substantially a same width and substantially a same length'.

However, Karnezos discloses in fig. 2 a package wherein the first and second chip scale packages 12/22 have substantially a same width and substantially a same length. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Karnezos as claimed for intended used. In addition, the Applicant has no support data, which convinces that the particular claimed configuration is significant or is anything more than one of numerous configurations a person of ordinary skill in the art would find obvious for the purpose of providing mating surfaces. In re Dailey 149 USPQ 47, 50 (CCPA 1966). See also Glue Co. v. Upton 97 US 3,24 (USSC 1878).

Response to Arguments

8. Applicant's arguments filed 16 Aug. 2005 have been fully considered but they are not persuasive. The Applicant argues that the Karnezos's metal layer 523 of the package 500 is connected to upper layer 421 of the bottom package 400. This is not persuasive because layer 523 is physically connected to 421 by wire 518, it is also electrically connected to the layer 423 of the bottom package through a via 422. Thus, such connection would read on the 'electrically connected' claim language. It is apparent that the Applicant may refer to the physical connection of the wire 192 from the connecting pads 166 to126 in fig. 4. It is noted that such features are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG PHAM
PRIMARY EXAMINER

Thao X. Le
Patent Examiner
16 Sept. 2005

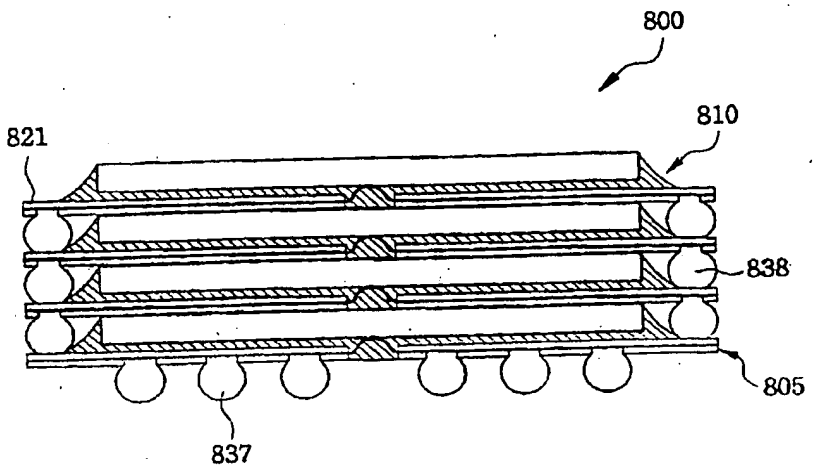
Dong-Ho LEE
STACK PACKAGE MADE OF CHIP SCALE PACKAGES
Attorney Docket No. 9903-074/Application No. 10/750,979

Replacement Sheet

1/1

FIG. 3

(Prior Art)



OK
TJ
9/15/05

FIG. 4